Power Efficient Comparator using Adiabatic Logic

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Abstract—*Main motive of this paper is to give a way to reduce the power dissipation of any digital circuit, since power dissipation is one of the main concern in digital circuits. This paper contains the design and simulation of comparator circuit which is simulated in NI MULTISIM software at 0.18 µm, 3V CMOS standard process technology with a frequency range of 200-800MHz. In this paper, a comparison of CMOS static comparator circuit with adiabatic logic and 2Pascl has been presented and it shows that the great amount of power saved in adiabatic logic as compared to static and 2Pascl.*

1. INTRODUCTION

Minimizing the power dissipation is a rising problems at all levels, such as circuits, logic, architecture, device technology and system levels. Development of a different low power solution is a daring job for the researches. Many approaches have been made by the researches to develop new methods to fulfill this low power objective. Out of this, one of the approaches is adiabatic logic [1]. Adiabatic logic is a new auspicious approach that has been created for low power digital circuits. One of the advantages of adiabatic logic circuits is that while invoking adiabatic logic circuits, it will decrease the switching noise of digital circuits [2].

This paper shows the comparative analysis of comparator circuit of its all three conditions. In this paper, power comparison of CMOS static, adiabatic array and 2pascal logics are shown.

1.1 Adiabatic Logic circuit

In this circuit, a clock signals called power clock has been used and instead of using a separate power supply for V_{DD} and clock [2], the clock signal can be used for the both purposes. Fig. 1 depicts a ramp type power clock supply. During the ramp up time, it permits the load capacitor energy to recycle again. This adiabatic cycling needs an adiabatic path between the logic circuit load and the power clock supply. It is possible to have the same path for charging, discharging process, but it may have separate paths for charging and discharging.

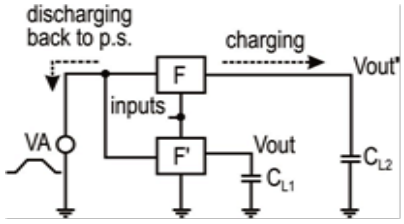

Fig. 1: Energy recovery charging and discharging

2. ADIABATIC SWITCHING TECHNIQUE

To minimize energy loss during the charging/discharging period, adiabatic switching is used [6]. In this adiabatic switching, at a constant current all the nodes are charged and discharged to reduce the amount of dissipated energy [3]. Here constant current source (I) are used to give charges to the load capacitance (C_L). On the contrary in conventional CMOS logic the load capacitance (C_L) is charged by constant voltage source. This is the basic difference between the adiabatic switching technique and CMOS static switching technique.

3. ADIABATIC ARRAY LOGIC

The adiabatic array logic composed of an array of transmission gates [7] to design an AND-plane and a wired OR plane which forms the second plane [5]. Depend on array logic the circuit drives a sinusoidal power supply, the power clock. This logic is presented in fig.2 [4]. AAL is used to implement circuits which basically have BOOLEAN terms based expressions.

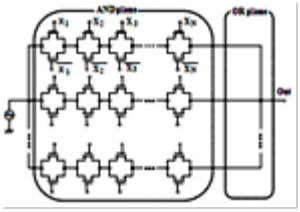

Fig. 2: Adiabatic Array Logic

4. CIRCUIT DESIGN AND SIMULATION

This section contains the circuit design and simulation of Comparator circuit which is designed and simulated in Multisim and with 0.18m standard CMOS process parameters, 200MHZ-800MHZ ranging frequencies and with a power clock of 3V.

4.1 Description

Comparator is a combinational logic circuit that compares two inputs binary and gives outputs to indicate which one has greater magnitude. It is useful in control applications where a binary number representing the physical variable being controlled is compared with a reference value.

Considering a 1 bit comparator having inputs A and B and the truth table is given below.

Table 1: Truth table of comparator

Inputs		Outputs		
A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

From the truth table, the Boolean expression can be written in terms of

For $A < B = \overline{A}B$

$$A = B = \overline{A}\overline{B} + AB = A \odot B$$

$$A>B = A\overline{B}$$

4.2 Circuit diagram

Fig. 3, 4, 5 represents the circuit design of three conditions of comparator circuit.

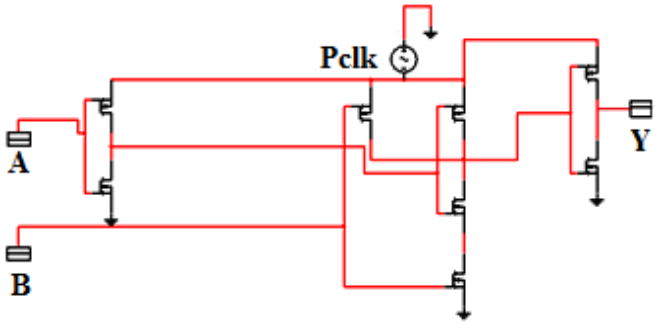

Fig. 3: Proposed Comparator circuit (A<B)

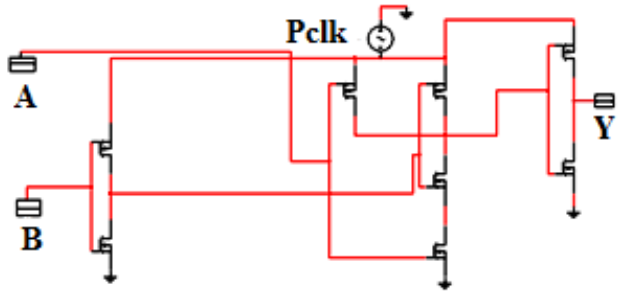

Fig. 4: Proposed Comparator circuit (A>B)

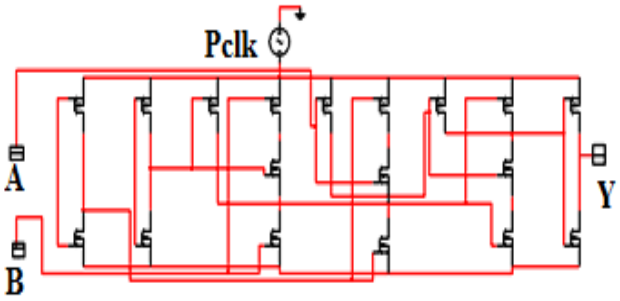

Fig. 5: Proposed Comparator circuit (A=B)

4.3 Simulated waveforms:

The following figures 6, 7, 8 of output waveforms were obtained as shown in below according to the simulation.

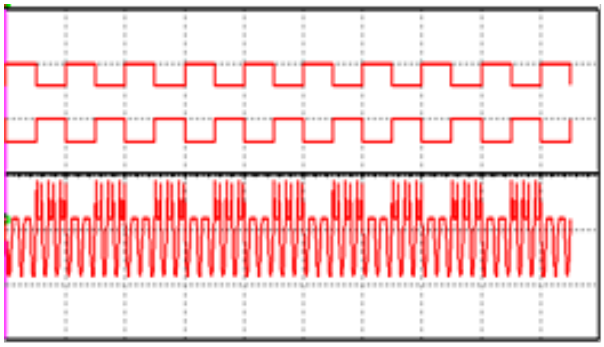

Fig. 6: Proposed Adiabatic Comparator input output waveform (A<B)

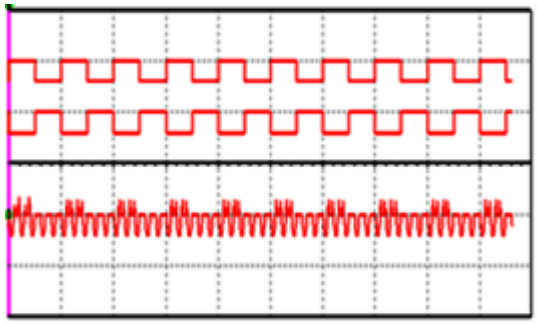

Fig. 7: Proposed Adiabatic Comparator input output waveform (A>B)

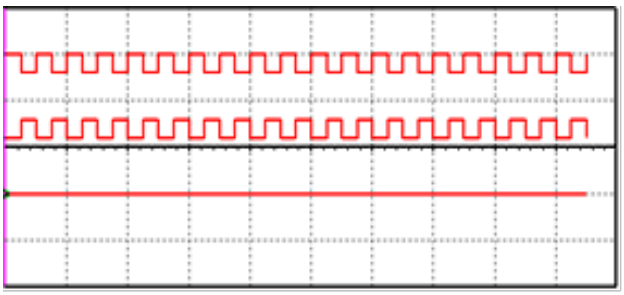

Fig. 8: Proposed Adiabatic Comparator input output waveform (A=B)

4.4 Power plot

Figures 9, 10, 11 portray the power plot comparison of comparator circuit, that is shown in NI-Multisim software at 0.18 µm, 3V CMOS standard process technology with W/L= 0.6 µm/0.18 µm for both PMos and NMos, $V_{PCLK} = 3V$ (peak-to-peak) and the required power plot was obtained.

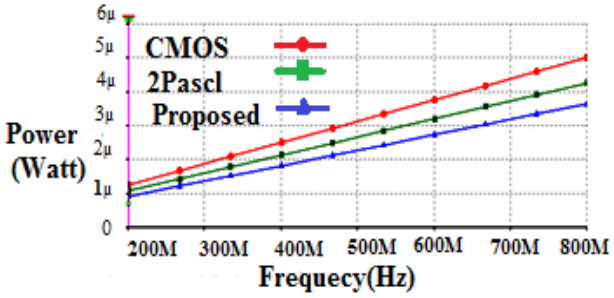

Fig. 9: Power plot comparison of Comparator (A<B)

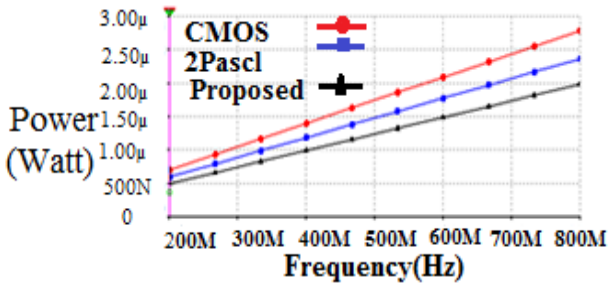

Fig. 10: Power plot comparison of Comparator (A>B)

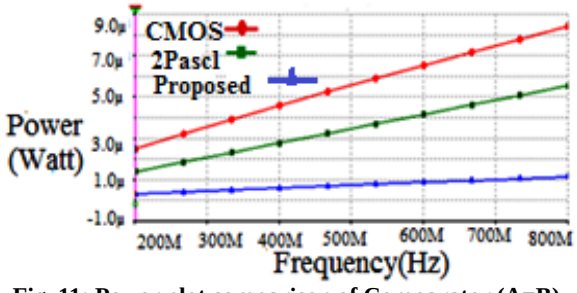

Fig. 11: Power plot comparison of Comparator (A=B)

4.5 Power dissipation analysis tables

The following tables 2, 4, 6 compares the performance of Comparator at two different frequencies , 200 MHZ and 400 MHZ in terms of transistor count, area per chip and most important the power dissipation.

Table 2: Performance analysis of various logic styles for Comparator (A<B)

LOGIC PARAMETER		STATIC	2PASCL	AAL
TRANSISTOR COUNT		8	14	8
AREA PER CHIP (μm^2)		0. 864	1.512	0. 864
TOTAL POWER DISSIPATION	AT 200 MHZ	1.256µ	1.066µ	909.518 n
	AT 400 MHZ	2.506µ	2.132µ	1.819µ

Table 3: Percentage power saving of proposed logic with respect to standard logic styles for Comparator (A<B)

2PASCL	STATIC
14.68%	27.41%

Table 4: Performance analysis of various logic styles for Comparator (A>B)

LOGIC PARAMETER		STATIC	2PASCL	AAL
TRANSISTOR COUNT		8	14	8
AREA PER CHIP (μm^2)		0.864	1.512	0.864
TOTAL POWER DISSIPATION	AT 200 MHZ	696.169 n	590.64 n	495.222 n
	AT 400 MHZ	1.392 µ	1.181µ	990.44 n

Table 5: Percentage power saving of proposed logic with respect to standard logic styles for Comparator (A>B)

2PASCL	STATIC
16.13%	28.84%

Table 6: Performance analysis of various logic styles for Comparator (A=B)

LOGIC PARAMETER		STATIC	2PASCL	AAL
TRANSISTOR COUNT		18	30	18
AREA PER CHIP (μm^2)		9	15	9

TOTAL POWER DISSIPATION	AT 200 MHZ	2.469µ	1.384µ	289.30 n
	AT 400 MHZ	4.592µ	2.767µ	578.59 n

Table 7: Percentage power saving of proposed logic with respect to standard logic styles for Comparator (A=B)

2PASCL	STATIC
79.08%	87.40%

*NOTE: Area per chip=W*L*Transistor count*

5. CONCLUSIONS

The researches include the power consumption of comparator circuit for three different conditions. The table shows the performance of different logic circuits and done the power comparison of three parameters with CMOS static, adiabatic logic array and 2pascal logic which was our main motive.

6. ACKNOWLEDGMENT

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